REMARKS

Claims 19-34 were pending in the application before this Office Action. Claims 19, 20, and 29 have been amended in this Response. Claims 19-34 are pending.

All amendments are made in a good faith effort to advance the prosecution on the merits. Applicants reserve the right to subsequently take up prosecution on the claims as originally filed in this or appropriate continuation, continuation-in-part and /or divisional applications.

Rejections under § 102

Claims 19-26 and 28 were rejected under 35 U.S.C. § 102(b) as anticipated by Intel's Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual. The Office Action states:

> 10. Referring to claim 19, Intel has taught a method, implemented in a computer system, of shifting a multi-word value comprising:
>
> a. performing a first shift operation on a first portion of the multi-word value to produce one or more overflow bits (Pages 4-16 and 4-17, pages 25-289 to 25-292, Bits are shifted out of the source register.);
>
> b. performing a second shift operation on a second portion of the multi-word value (Pages 4-16 and 4-17, pages 25-289 to 25-292, Bits are shifted in the destination register.),
>
> c. where the second shift operation comprises:
>
> i. producing a shift result; and concatenating the shift result and the overflow bits (Pages 4-16 and 4-17, pages 25-289 to 25-292, A lower portion of bits of the destination are concatenated with the bits shifted out of the source register.) and
>
> ii. where the second shift operation is a multi-precision shift instruction (pages 25-289 to 25-292, SHRD and SHLD are double (or multi) precision shift right/left instructions. The second shift operation shifts by 64 bits or more, therefore the second shift operation is multi-precision shift instruction.) and where the first shift instruction and

> second shift instruction are performed sequentially (The first operation produces overflow bits. The second operation concatenates a shift result with the overflow bits produced from the first operation. Therefore, the second operation must be sequential to the first operation since the second operation cannot be performed until the first operation has completed and produced the overflow bits.).

Office Action, pages 4-5.

Applicants disagree. Applicants' first and second shift operations are separate shift operations that are performed sequentially. Intel does not disclose such a method. Instead, Intel discloses a single shift operation. For example, Intel states at page 25-289 that "[t]he SHLD instruction shifts the first operand provided by the r/m field to the left as many bits as specified by the count operand. The second operand (r16 and r32) provides the bits to shift in from the right (starting with bit 0)." Intel does not support the Office action's assertion that "[t]he first operation produces overflow bits. The second operation concatenates a shift result with the overflow bits produced from the first operation. Therefore, the second operation must be sequential to the first operation since the second operation cannot be performed until the first operation has completed and produced the overflow bits." Intel does not disclose Applicant's "first shift operation" and "second shift operation." Instead, Intel discloses a single operation where the first operand is shifted and the fill is provided from the second operand. The Office action's assertion regarding the operation of Intel are an application of Applicants' claimed method to achieve the same end as Intel. Intel, however, does not disclose each element of claim 19. Applicants have further added the limitation that "the one or more overflow bits are stored in an overflow register prior to concatenation with the shift result," in an attempt to make this distinction more clear.

Claim 19 and dependent claims 20-28 are therefore patentable over Intel. Applicants respectfully request that the rejection be withdrawn.

Rejections under § 103

Claims 27 and 29-34 were rejected under 35 U.S.C. § 103(a) as unpatentable over Intel and U.S. Patent No. 6,314,200 to Silverbrook.

First, claim 27 depends from claim 18, which Applicants have shown to be patentable above. Applicants therefore respectfully request the withdrawal of the rejection of claim 27.

> The Office Action states that:
>
> 22. Referring to claim 29, Intel has taught a processor for processing multi-precision shift instructions, comprising:
>
> a. a program memory for storing instructions including at least one multi-precision shift instruction (Page 3-2, lines 1-3, The program code, or instructions, are stored in the memory. SHLD and SHRD instructions are multi-precision shift instructions, see 4-16, 4-17 and 25-289 to 25-292);
>
> b. a program counter for identifying current instructions for processing (page 3-15, section 3.3.5, Instruction Pointer), and
>
> c. a shifter for executing shift instructions (Page 4-16 and 4-17), including the at least one multi-precision shift instruction (Pages 4-16 and 4-17, SHLD and SHRD), the shifter including:
>
> i. one or more carry registers for storing values shifted out of sections of the barrel shifter (Page 4-16 and 4-17, CF); and
>
> ii. logic for concatenating values stored in one or more carry registers with values in the shifter (pages 4-16 and 4-17, pages 25-289 to 25-292, A lower portion of bits of the destination are concatenated with the bits shifted out of the source register.); and
>
> d. where the barrel shifter is operable to shift a multi-word value (Pages 4-16 and 4-17, SHLD and SHRD shift doubleword operands), and where when shifting a multi-word value the shifter:
>
> i. executes at least one shift instruction to:
>
> (1) load a first operand into a section within the shifter, where the first operand is a first portion of the multi-word value (Pages 4-16 and 4-17, The

source operand is loaded into the source register.); and

(2) generate one or more overflow bits (Pages 4-16 and 4-17, Bits are shifted out of the source register.); and

ii. executes at least one multi-precision shift instruction fetched from the program memory (Pages 4-16 and 4-17, The SHRD and SHLD instruction are executed.) to:

(1) load a second operand into a section within the shifter, where the second operand is a second portion of the multi-word value (Pages 4-16 and 4-17, The destination operand is loaded into the destination register.);

(2) shift the operand; concatenate the operand with one or more of the overflow bits (Pages 4-16 and 4-17, A lower portion of bits of the destination are concatenated with the bits shifted out of the source register.); and

(3) output the shifted value (Pages 4-16 and 4-17, The result is stored back into, or output to the destination operand.).

Office Action, pages 8-10.

Applicants respectfully disagree. Like claim 19, claim 29 requires the execution of two separate shift operations. Specifically, claim 29 requires that the processor "executes at least one shift instruction to . . . generate one or more overflow bits" and "executes at least one multi-precision shift instruction . . . to . . . shift the operand; concatenate the operand with one or more of the overflow bits." As discussed above with respect to claim 19, Intel does not disclose both of these shift operations. Applicants have also added the limitation of "storing the one or more overflow bits in an overflow register" in an attempt to clarify the distinctness of the two shift operations. Claim 29 and dependent claims 30-34 are therefore patentable over Intel and Silverbrook.

SUMMARY

Should the Examiner have any questions, comments or suggestions in furtherance of the prosecution of this application, the Examiner is invited to contact the attorney of record by telephone or facsimile.

If the Commissioner deems any additional fee is due, the Commissioner is hereby requested to accept this as a Petition therefore, and is authorized to charge any fees due, including any fees for an extension of time, to Baker Botts L.L.P. (formerly, Baker & Botts, L.L.P.) Deposit Account number 02-0383, Order number 068354.1439.

Respectfully submitted,

BAKER BOTTS L.L.P. (031625)

/Bradley S. Bowling/
Bradley S. Bowling
Reg. No. 52,641
Baker Botts L.L.P.
910 Louisiana
Houston, Texas 77002
Telephone: (713) 229-1802
Facsimile: (713) 229-7702
ATTORNEY FOR APPLICANTS

Date: March 2, 2007